Design of a High-Precision ADC Test Platform Integrating STC12C5A60S2 Microcontroller and XGBoost-Based Dynamic Performance Estimation

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In this paper, a high-precision analog-to-digital converter (ADC) test platform integrating both hardware and software is developed to enable accurate evaluation of ADC performance. On the hardware side, the platform employs the STC12C5A60S2 microcontroller in conjunction with the AD9833 signal generator, supported by amplification and filtering circuits, to ensure stable signal acquisition. On the software side, static parameters are extracted through statistical and time-series analysis, while a gradient boosting regression model based on XGBoost is utilized to estimate key dynamic performance metrics such as total harmonic distortion (THD). The proposed system supports both static and dynamic ADC testing and achieves high estimation accuracy with low complexity. Experimental results demonstrate that the platform can estimate THD with errors within ±2 dB for 85% of the test samples, and within ±3 dB for 92%, outperforming traditional FFT-based methods. Moreover, the effective number of bits (ENOB) deviation remains within ±0.5 bits across diverse conditions. This work provides a cost-effective and extensible solution for ADC characterization, suitable for both laboratory testing and industrial applications.

Povzetek: Članek predstavi platformo za testiranje analogno-digitalnih pretvornikov, ki združuje nizkocenovno strojno opremo z modelom XGBoost za ocenjevanje statičnih ter dinamičnih parametrov.

1 Introduction

Information acquisition and processing have become the core of modern information technology, social development, and scientific and technological progress plays an important role. Sensors as the information acquisition and processing system in the front-end components, directly facing the object being measured, become a world of today's attention to the rapid development of high-tech [1], but also an important symbol of the rapid development of contemporary science and technology [2]. It is the realization of modern measurement and automatic control (including remote sensing, telemetry, and remote control) of the main links, that are the source of the modern information industry, but also the information society depends on the existence and development of the material and technological basis [4]. Now sensing technology and information technology, computer technology, side by side to support the whole modern information industry of the three pillars. In particular, the development of microelectronics technology, microcomputer technology, and information processing technology, made the sensor small in size, low cost, multi-function, and integrated direction [5]. At present, from universe exploration, marine development, environmental protection, and disaster forecasting to the life sciences, including every modern science and technology research as well as people's daily lives [6], etc., almost none of them are closely linked with sensors and sensor technology. Therefore, it is no exaggeration to say: that no sensor and its technology will not have the rapid development of modern science and technology.

A/D converter to convert analog into digital quantities, microcontroller to carry out data processing [7]. With the rapid development of ultra-large-scale integrated circuit technology, a large number of different structures, and performance varies A/D converter chips should come into being [8]-[9]. For the designer, only a reasonable choice of chips can be. Now part of the microcontroller chip is also integrated into the A/D converter, the number of bits for the 8-bit, 10-bit, or 12-bit, and the conversion speed is also very fast, but in the case of the chip can’t meet the needs of the A/D converter, or the need to expand. Therefore, the basic method of external expansion of the A/D converter should be mastered four. This paper uses the AD9833 as an AWD converter chip for A/D conversion simulation experiments.

Analog-to-Digital Converter (ADC) test is divided into static test and dynamic test [10]-[11]. Static test research earlier now has a more perfect test method, but the static test can’t reflect the dynamic characteristics of

the ADC [12], so the general choice of ADC dynamic test method, can reflect the performance of the ADC more perfectly.

Through the static parameter testing process estimate the noise power, and then find out the Effective number of bits (ENOB) and Signal-to-noise and distortion ratio (SND) of the converter. In 2006, Hsill-Wen Ting et al. carried out a study on the correspondence between the nonlinear characteristics and harmonics and established the integral nonlinear characteristics and the harmonic relationship. In 2006, Hsill-Wen Ting et al. investigated the correspondence between the nonlinearity characteristics and harmonics and established a mathematical expression between the integral nonlinearity (INL) and the noise power, which can obtain the effective number of bits and the integral nonlinearity by calculating based on the histogram of the code density obtained under the excitation of a sinusoidal signal. 2011 Duan Jingbo et al. investigated the correlation between input noise and Differential nonlinearity (DND) of the measured device based on the statistical analysis. Differential nonlinearity (DNL), and based on this, the noise power is estimated by analyzing the noise contained in the DNL, and then the SND and ENOB are derived [13].

Harmonic distortion parameters are estimated using a static parametric testing procedure. The integral nonlinearity can describe the transfer characteristic curve of an analog-to-digital converter [14], while under the excitation of a larger amplitude sinusoidal signal, the nonlinearities inside the converter act periodically on the output as shown in Fig. 1, and appear as harmonic components in the form of harmonic components in the spectrum of the output signal. Based on this principle, Jingbo Duan et al. proposed in 2012 to sample the INL curve with the Sine signal, which is equivalent to the output waveform of the converter in the dynamic parameter test, and the harmonic correlation relationship has been obtained by spectral analysis of this waveform and the corresponding dispersion-free dynamic range and total harmonic distortion parameter indexes [15]. In applications that require low-frequency measurement of spectral performance, this method can achieve the same measurement accuracy as traditional test methods [16]. Table 1 presents the similarities and differences among these research works.

Table 1: Related works summary

Reference	Test Type	Architecture	Performance Metrics Reported	Limitations
Duan & Chen (2011) [13]	Static + Dynamic	Code histogram-based + FFT	ENOB, SNR, DNL, INL	Low dynamic estimation accuracy
Janik & Fresnaud (2007) [14]	Dynamic	Spectral method	INL, THD	Lacks flexibility for real-time test
Duan et al. (2012) [15]	Dynamic	INL-sampling with sine excitation	THD, SFDR, ENOB	Complex hardware dependency
Wei et al. (2023) [11]	Static	LabVIEW + Integrated ADC	DNL, INL, Offset	No support for machine learning
Proposed (This work)	Static + Dynamic	STC12C5A60S2 + FFT + XGBoost	THD (±2 dB, 85%), ENOB (±0.5 bits)	Improves accuracy with low-cost microcontroller, interpretable ML model

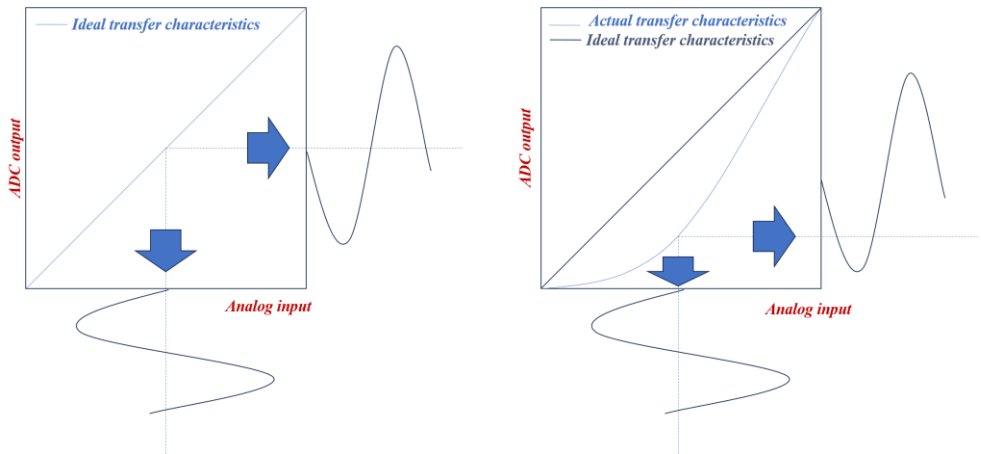

Figure 1: Schematic representation of the effect of nonlinearity on ADC functionality

The function of an analog-to-digital converter is to convert an analog signal, which is continuous in both time and amplitude dimensions, into a digital signal with discrete amplitude and time [17]. The static and dynamic parameters are the two core performance parameters of the converter [18], in which the static parameters are mainly used to describe the transfer characteristic curve of the ADC, including Integral

nonlinearity (INL), Gain error (GE), Differential nonlinearity (DNL) and Offset error (OE), the dynamic parameters are related to the spectral performance and measure the extent to which the ADC can reproduce a sinusoidal signal as a digital signal under its excitation. They mainly include Signal-to-noise-and-distortion ratio (SND), Total harmonic distortion (THD), Effective number of bits (ENOB), Spurious-free dynamic range (SFDR), and Signal-to-noise ratio (SNR).

ADC is one of the core devices in modern electronic systems, responsible for converting analog signals into digital signals for subsequent processing and analysis [19]-[20]. Accurate evaluation of ADC performance is critical in applications requiring high precision, such as medical imaging, precision instruments, and communications [21]. However, current ADC test platforms have trade-offs between cost, accuracy, and scalability, and it is difficult to comprehensively evaluate their static and dynamic performance characteristics.

To address these issues, this paper proposes a novel ADC test platform that combines the co-design of hardware and software and is capable of meeting the test requirements of high accuracy and flexibility. The hardware part of the platform adopts the STC12C5A60S2 microcontroller and AD9833 chip to support data acquisition and processing; the software part realizes signal analysis through the FFT algorithm and accurately estimates dynamic performance through the dynamic parameter gradient boost regression model. The research in this paper aims to provide an efficient and reliable solution for ADC testing [22]-[23].

This paper combines the feature extraction methods of nonlinear curves with principal component analysis and time series research, compares and determines the optimal feature combinations, and the optimal hyperparameters of each model, and analyzes the significant differences between various estimation models based on an understanding of the algorithmic principles and the characteristics of dynamic parameter estimation problems, in order to determine the optimal model. Furthermore, it quantitatively evaluates the contribution degree of specific feature variables within the model interpretation framework, thereby improving model transparency. Finally, the modeling and correlation analyses in this study were performed on the Jupyter Notebook platform using open-source libraries in Python 3.7, including NumPy120,3, Pandas1.3.4, Scipy I.7.1, Matplotlib3.4.3, TensorFlow2,80, sHAP041.0, xgboost1.7.0, and others. This research aims to answer: (1) Can machine learning improve dynamic performance estimation in ADC testing? (2) What is the accuracy improvement of XGBoost-based THD prediction compared to traditional FFT analysis? Success is defined by reducing THD prediction error below ±2 dB for >85% of test samples.

2 Hardware designs

2.1 STC12C5A60S2 microcontroller with AD9833 chip

This design uses the STC12C5A60S2 microcontroller as the control core to control and configure the AD9833. Through the key can directly enter the signal frequency and amplitude, as well as waveform type switching, very easy to use. AD9833 output voltage is only 3V, and the actual use of the waveform voltage is often larger, so it also needs to be amplified. The design of the amplifier circuit AD8397 amplifies the voltage to reach between 0.1V and 5V adjustable so that the signal gets a larger power. At the same time, the LCD shows the parameters of the indicators. The system hardware block diagram is shown in Figure 2.

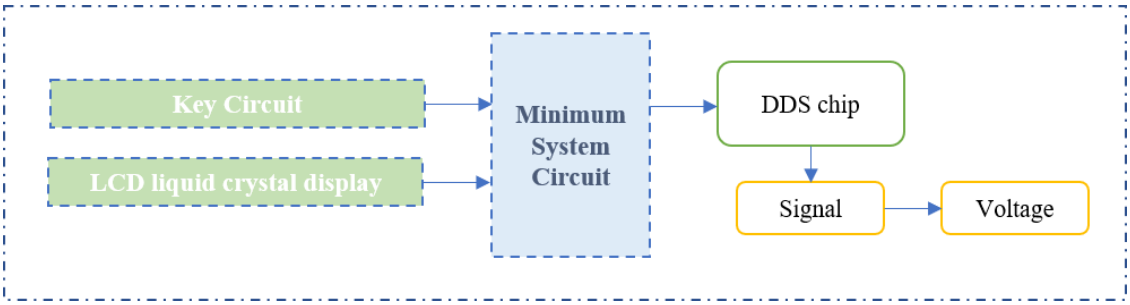

Figure 2: System hardware block diagram

STC12C5A60S2 is a new generation of 8051 microcontrollers, containing a central processing unit (CPU), program memory (Flash), data memory (SRAW), timer/counter, UART serial port, high-speed A/D conversion, SPI interface, other modules. Support for serial program burning and the development of microcontroller equipment requirements are relatively low, the time is relatively shortened and cost-effective. The microcontroller minimum system clock circuit using a crystal oscillator 11.0593Hz, capacitance selection of 20pf capacitors. Because the function signal generator needs to continuously output waveforms and does not need to often reset this minimum system circuit does not specifically draw a reset circuit.

AD9833 is a high-precision, low power consumption, simple structure and small size and has a serial interface function of the DDS chip, produced by ADI, its output signal control, such as frequency and

phase can be programmed to control the realization of the AD9833 chip power supply voltage range of 2.3V ~ 5.5V, the output waveform through the VOUT pin.SDATA input, FSYNC When SDATA is input, FSYNC must be low, and the data is sent to the shift register of AD9833 after 16 falling edges of SCLK to load the data bits. The waveform output from the AD9833 chip depends on the control bits OPBITEN(D5) and Mode(D1) in the control register of the controller. If the content in the AD9833 control register needs to be changed, the D15 and D14 positions go low. When the phase register is written D15 and D14 are set high and D13 specifies which phase register is written.

2.2 Amplification circuit design

To meet the required output signal amplitude of up to 5 V, the analog output of the AD9833 signal generator, which is limited to approximately 0.6–0.7 V peak-to-peak, is amplified using a high-output-current operational amplifier, the AD8397. A standard non-inverting amplifier configuration is adopted to preserve signal polarity and minimize phase distortion.

The gain of a non-inverting amplifier is defined by the following transfer function:

$$V_{out} = (1 + \frac{R_f}{R_g})V_{in}$$

where Rf is the feedback resistor and Rg is the resistor connected between the inverting input and ground. In our design, both Rf and Rg are set to 10 kΩ, resulting in a voltage gain of:

$$V_{out} = (1 + \frac{10k\Omega}{10k\Omega})V_{in} = 2V_{in}$$

This amplification factor effectively boosts the signal amplitude to a usable level for ADC testing. The AD8397 is selected due to its high current drive capability (up to 310 mA) and wide bandwidth, ensuring minimal distortion and accurate amplification even at higher frequencies.

The previously ambiguous statement "inverted input through the resistor R4 ground" has been clarified in this context as the resistor Rg connected between the inverting input of the op-amp and ground. The non-inverting input receives the filtered output of the AD9833 signal generator, ensuring signal fidelity throughout the amplification stage.

2.3 Filtering circuit design

To improve signal integrity and suppress high-frequency noise components that may affect the accuracy of ADC conversion, a basic first-order low-pass filter is added after the amplification stage. This filter consists of a series resistor and a parallel capacitor to ground, forming a simple RC structure with a cutoff frequency selected based on the maximum test signal frequency. In our implementation, the resistor and capacitor values are chosen to yield a cutoff frequency of approximately 1 kHz, which effectively attenuates high-frequency interference while preserving the essential signal content required for ADC evaluation. The addition of this filtering stage ensures a cleaner input waveform to the ADC under test and enhances the reliability of static and dynamic parameter extraction in subsequent analysis stages.

3 Hardware architecture system design for ADC test bench

3.1 High-precision data processing system

The test daughter board is designed according to different models of ADC chips to meet their respective test requirements [24], in the test, only need to replace the top layer of the ADC test daughter board can complete the test, which makes the data converter test platform with communication. The structure of the ADC test daughter board block diagram is shown in Figure 3, the circuitry includes the ADC chip, signal inputs, clock inputs, Barron circuit high-speed data interface, etc. Among them, the high-speed data interface is the interface to communicate with the FPGA data processing system. One of the high-speed data interfaces for the test daughter board and FPGA data processing system communication interface, through the interface to complete the transmission of sampling data: when the ADC chip input signal for differential signals, the need for a balun circuit will be converted to differential signals to the ADC chip input pins.

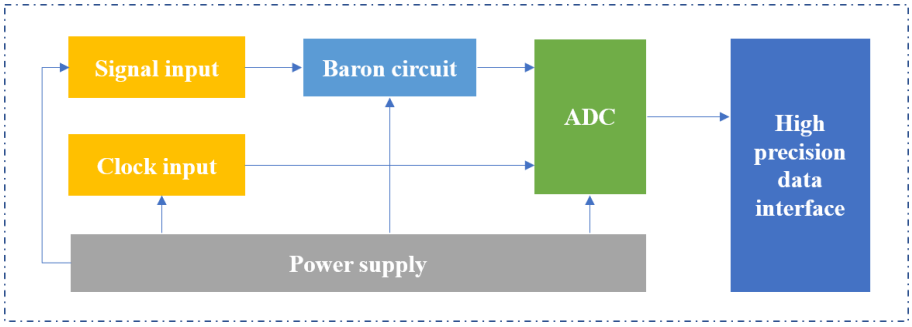

Figure 3: ADC test daughterboard block diagram

The high-speed data processing system of the test platform can directly receive the output signal of the ADC [25], so in the hardware design of the test daughter board, it is only necessary to ensure that the ADC chip can work normally and stably output signals, and the output signals can be directly transmitted to the high-speed data processing system through the high-speed data interface.

High-speed data processing system to complete the control of the top ADC chip and ADC output data acquisition, but also to complete the data processing and transmission, high-speed data processing system functional block diagram shown in Figure 4, by the FPGA chip, crystal circuit, high-spee

d data interface, JTAG (Joint Test Action Group) circuit, Gigabit network interface circuit, and other components.

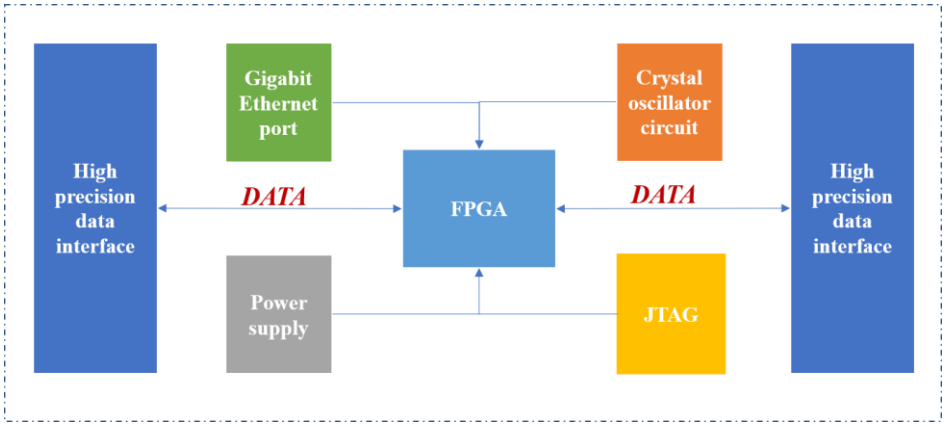

Figure 4: Functional block diagram of high-precision data processing module

The core chip of the high-speed data processing system uses Xilinx Virtex6 series model XC6VLX240T FPGA, which has 720 input/output pins, 416 36kb block memories, and can complete the acquisition of ADC output signals, the acquisition of data processing and transmission functions. The JTAG circuit in the high-speed data processing system provides the function of downloading and debugging for the FPGA chip, which can download the program into the FPGA through ISE software and complete the online debugging by using the Chipscope function to check the status of the selected signal when the FPGA is running.

The control system Is the control center of the whole test platform, Ih accomplishes the following tasks:

(1) establish communication with the high-speed data processing system, complete the programming function of the high-speed data processing system, monitor and control the status of the high-speed data processing system, as well as

state monitoring and control functions, as well as to complete the transmission of ADC sampling data.

(2) Establishing communication with the host computer, completing the control of the whole test platform by receiving commands from the host computer, and uploading the sampling data to the host computer.

(3) Establish communication with the chip test daughter board, complete the read/write operation of the chip registers in the test daughter board module, and then complete the chip initialization and other related operations. The ARM control system establishes a communication connection with the upper computer through the network port and establishes a communication connection with the upper high-speed data processing system through the high-speed data interface, which completes the control of the whole test platform, including the configuration of the ADC chip, the status control of the high-speed data processing system, the control of the ADC chip, the status control of the ADC chip, and the control of the ADC chip status. Data processing system state control, ADC sampling data transmission, etc. The ARM control system is developed around Samsung's S3C6410 processor, which can run the Linux system, has a very complete bus architecture, and operates at a fast speed and high efficiency.

3.2 ADC test bench solution

The proposed test platform is developed based on a prior ARM-FPGA implementation. In the original system, an ARM processor served as the control module, coordinating ADC data acquisition and system configuration. However, due to the high operating frequency of the ARM core, electromagnetic interference was observed, which affected the accuracy of high-precision ADC measurements. To mitigate this, the ARM control module was replaced with an MSP430 microcontroller in the updated platform design. ARM-FPGA data converter test platform has been well realized ADC chip test, but due to the high frequency of ARM operation, the test process will produce a small part of the interference signal, these interference signals are extremely small, but in the high-precision ADC test will be crosstalk to the ADC output signals, for the test results of the impact of some. Therefore, to ensure the accuracy of the test results of high-precision ADC chips, the elimination of interference has become the primary solution to the problem.

Low-power microcontrollers due to their low operating frequency, have the characteristics of small power consumption, the external electromagnetic radiation is much smaller than ARM, and can solve the interference problems brought by the ARM platform. At the same time, it has a powerful expansion function and can meet the basic needs of the test platform control system, so it was selected as the implementation program of this paper. The new MSP430-FPGA data converter test platform is improved and completed based on the original ARM-FPGA data converter test platform design of the three-layer stacked circuit board design, so that the original design of the test daughter board module and high-speed data processing system is completely retained, and only need to change the design of the MSP430 control system and the upper computer control software interface, which reduces the workload.

Therefore, the MSP430-FPGA data converter test platform retains the original test platform architecture, replaces the ARM control system with the MSP430 control system, re-designs the hardware board-level circuitry to realize the basic needs of the control system, develops software around the low-power microcontroller module, and develops a Bluetooth wireless communication module based on wired communication with the upper computer to extend the communication between the test platform and the host computer. The Bluetooth communication module can be embedded into the msp430 control system to work, establish communication with the control system through the SPI communication interface, establish communication with the host computer based on the Bluetooth wireless communication protocol, and be able to provide Bluetooth wireless communication connection when the wired communication method is not connected. At the same time, the Bluetooth wireless communication connection reduces the common ground interference between the host computer and the test platform, further reducing the impact on the test results.

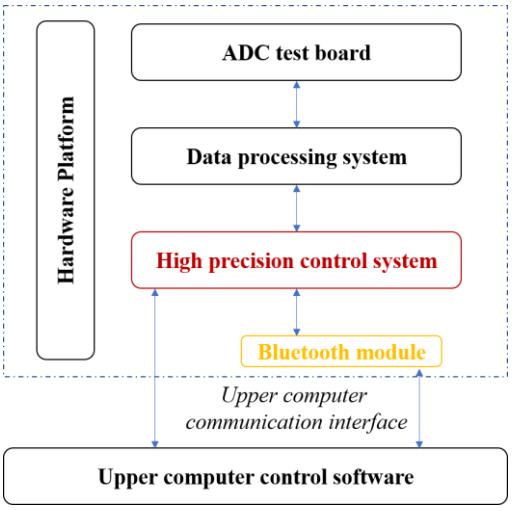

Figure 5: Data converter testbed architecture

The architecture of the data converter test platform Is shown In Figure 5, where the MSP430 control system replaces the original ARM control system, establishes a communication connection with the hardware platform's upper-level high-speed data processing system through the high-speed data interface, and establishes a communication connection with the host computer through the host computer communication interface. The host computer control software sends control commands to the control system through the host computer communication interface, and the control system executes the commands and then controls the data processing system and the ADC test daughter board through the high-speed data interface so that they are in the corresponding test state. When the ADC chip completes the data conversion, the collected data are processed by the data processing system and transmitted to the control system through the high-speed data interface, and then the control system uploads them to the control software through the communication interface of the host computer, and the control software finally processes the data and calculates the performance parameters to get the test results.

To clarify the relationship between the signal generation and ADC testing components, this work adopts a modular system design in which the signal generator module—comprising the STC12C5A60S2 microcontroller, the AD9833 direct digital synthesis (DDS) chip, and an AD8397-based amplification circuit—acts as the excitation source for the ADC under test. The analog signal produced by this module is transmitted directly to the input of the ADC device, such as the ADC0804, which is mounted on a replaceable test daughterboard. This daughterboard interfaces with the high-speed FPGA-based data processing unit, which captures the ADC output and forwards the sampled data for subsequent analysis.

By separating the signal generation from the data acquisition and processing components, the system minimizes electromagnetic interference and facilitates better control over input conditions. The overall platform, coordinated by the control module and host software, supports full-loop operation for both static and dynamic testing of ADC performance. This integration ensures that the signal chain from excitation to parameter estimation remains coherent, accurate, and adaptable to different ADC configurations.

In this design, the networked communication interface between the host computer and the original platform is also changed. The changed communication interface of the host computer consists of two ways, one is a wired connection based on a USB interface and the other is a wireless connection based on Bluetooth communication module. The Bluetooth communication module establishes a communication connection with the control system through the Serial Peripheral Interface (SPI) communication interface, and the wireless connection can solve the common electrical interference that may be introduced when the host computer and the test platform are directly electrically connected, and further improve the performance of the test system.

4 Parameter estimation algorithm design and implementation

4.1 Static performance feature extraction method design

The gain error offset error, and DNL and NL curve data provide a complete picture of the static characteristics of the system. These parameters are obtained by further calculations based on the density histogram [26]. The nonlinear curves can be considered as sampling information in a particular distribution, and this particular distribution shows different dynamics with different dynamic parameters. Therefore, the features describing this distribution are extracted from the nonlinear curve, which can effectively characterize the ADC dynamic parameters.

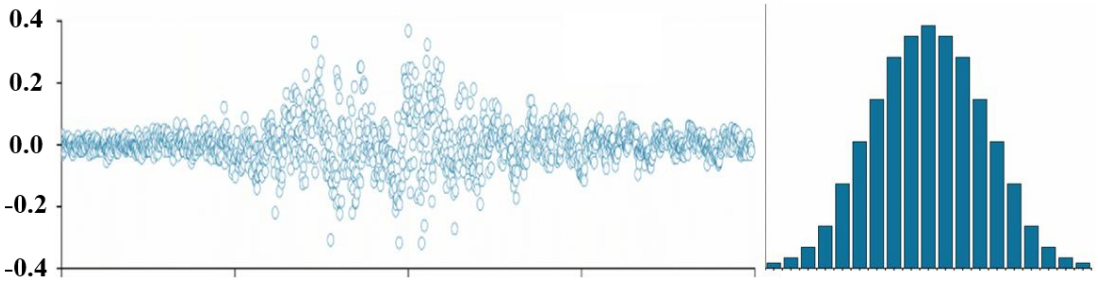

Figure 6. DNL curves and their statistical histograms

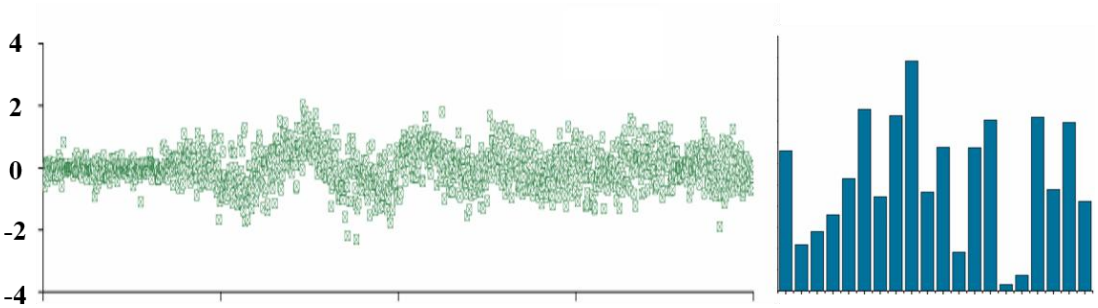

Figure 7: INL curves and their statistical histograms

Figures 6 and 7 show a set of measured integral nonlinearity (INL) and differential nonlinearity (DNL) curves of the ADC0804, along with their corresponding statistical histograms. From Fig. 6, it can be seen that the DNL curves can be approximated as a section of white noise, i.e., the sequence is completely random without some kind of periodicity or trend, and the correlation of the integral nonlinear errors between different points is low, making it difficult to predict another point based on one point. This is in general agreement with the conclusion of Jinbo Duan et al. in the literature [15] that the differential nonlinear curve can be regarded as a smooth sequence. As can be seen from Fig. 7, the NL curve has the following characteristics: (1) the data in the series have some kind of trend, and the correlation between the two points that are closer together is stronger: (2) the values of the points with larger intervals in the series have a certain degree of randomness. A time series is a string of data lined up in chronological order. Analyzing the characteristics of time-series data by studying the dependencies between the data within the time series is known as time-series analysis in academic circles. Time series modeling can be used to observe trends in monitoring data over long periods. Combining the characteristics of the NL and DNL curves mentioned above, it can be found that the static nonlinear curve of ADC is very similar to the non-stationary time series and the stationary time series in time series analysis. Therefore, time series are used here for feature extraction of nonlinear characteristic curves of analog-to-digital converters.

The most commonly used method for feature extraction of smooth time series Is statistical analysis. Therefore, in this work, the correlation index in statistical analysis is adopted as the feature extraction method for the integral nonlinear and differential nonlinear curves to fully portray the static nonlinear characteristics while reducing the feature space. In this paper, we first consider the common statistical features related to nonlinear curves: mean value, root mean square value, standard deviation, and other eight statistical indicators. These indicators portray the distribution of nonlinearity from different perspectives.

Skewness, g1 describes the direction and degree of the distribution shift. If g1>0, the distribution is right-skewed and vice versa. A larger |g| means that the more skewed the distribution is. Kurtosis, g2 is used to characterize the steepness of a statistical distribution as shown in Figure 8, the larger g2, the steeper the distribution. The kurtosis of a normal distribution is equal to 3. The curve of the distribution is “flatter” when

the kurtosis is less than 3, and "steeper" when it is greater than 3.

According to the above analysis, there is some information redundancy in the integral nonlinear curve. Principal Component Analysis can analyze and reduce the dimensionality of nonlinear curves, and its core idea is to find a direction so that the original data are scattered as much as possible in the projection direction, and then map the original data to this direction by orthogonal transformation. At this point, this direction contains the most information about the sample data set. Finally, by retaining the large variance dimension and ignoring the small variance dimension, PCA can reduce the dimensionality of the data while retaining as much information as possible about the differences between the samples, and the feature dimensions obtained in this way are orthogonal (uncorrelated). Moreover, it has been proved that PCA transformation is the best orthogonal transformation.

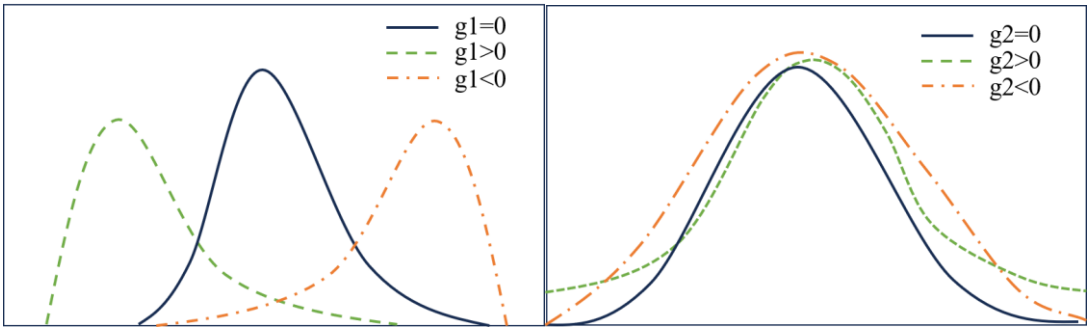

Figure 8: Skewness and kurtosis schematic

Figure 9 illustrates the first 16 principal components of the integral nonlinear curve and their percentage of explainable variance, where the bar represents the percentage of explainable variance of the sample along the direction of that principal component, and the curve is a cumulative sum of the bars representing the percentage of explainable variance of the data over the space tensored by the first n principal component directions. As can be seen in Figure 10, the interpretable variance of the data reaches 84.7% in the 1st principal component direction alone, and the sum of the variance in the first three principal component directions reaches 89.5%. In addition, the percentage of the explainable variance of the principal components at the back of the ranking begins to gradually converge to zero. This means that not much information is lost by discarding the later principal components. To limit the complexity of the model, the work in this chapter selects the first 48 principal components as the feature input variables of the THD estimation algorithm based on machine learning, and the cumulative explainable variance reaches 97%.

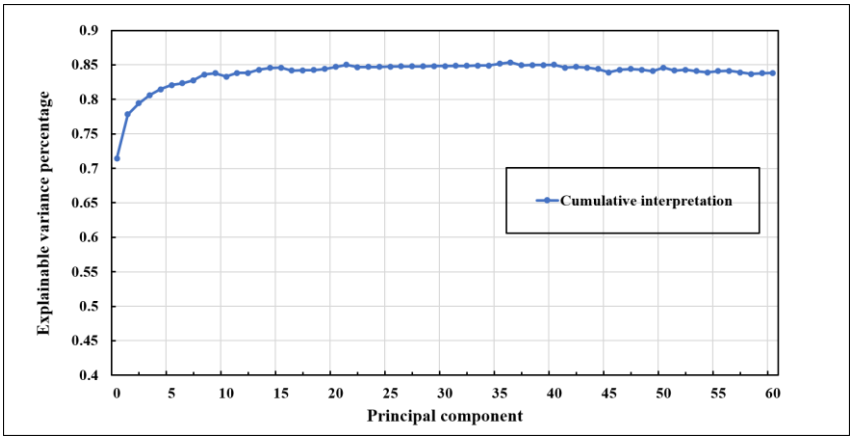

Figure 9: Percentage of variance explained by principal components

4.2 Dynamic parameter gradient boosting tree regression model

In this study, the problem to be solved is to estimate the THD parameters of the same but with different performance parameters ADCs with the input features of each machine learning model as X= [GE, OE, INL-PCA-i, INL-statistical features, DNL-statistical features], where INL-PCA-i stands for the ith principal component of the NL with i=O,1,2,47. This belongs to the regression learning problem.

Boosting is a machine learning technique that integrates multiple weak learners for regression and classification problems. If during training, each iteration of the model generates a weak learner based on the gradient direction of the loss function to complement the

original model, fit the residuals between the true values and the output of the original model, and ultimately enhance the learning capability by integrating multiple weak learners, then the whole model can be called a Gradient boosting machine (GBM).

The XGBoost (eXtreme Gradient Boosting) model was first proposed in 20l6 by Chen and Carlos Guestrin [27] first proposed a model for implementing gradient-boosting regression trees. At each iteration of XGBoost, trees are added to the existing model, and the scores of multiple trees are eventually summed up as the final model inputs.XGBoost generalizes the loss function by a 2nd-order Taylor series expansion, so that the specific form of the loss function can be disregarded, and decoupling model optimization from loss function selection is realized This increases the generalizability of the model. Compared to other classical machine learning algorithms, XGBoost shows higher prediction accuracy and faster processing time in many domains, as well as lower computational cost and complexity. These properties apply to dynamic parameter estimation problems.

To get the best performance from XGBoost, this work initializes all the parameters of the model concerning Table 1 and uses GridSearchCV to perform an exhaustive search of the hyperparameters with specified parameter values. Table 2 shows the optimal hyperparameters searched by GridSearchCV, and the effect of each hyperparameter on the output of the model is analyzed below. This integration of machine learning into embedded systems for real-time parameter estimation follows similar strategies reported in recent research [28].

Table 2: Hyperparameter optimization space and optimal values for XGBoost

Model parameters	Starting value	Search space	Grid Search Optimization
n_estimators	100	[100,150,200,250,300]	200
γ	0.47	[0,0.2,0.5,0.8,1.0]	0
max depth	4	[2,3,4,5]	5
learning_rate	0.16	[0.03,0.05,0.08,0.1]	0.06
colsample_bytree	0.82	[0.6,0.7,0.8,0.9]	0.8
min child weight	1	[1,2,3,4,5,6]	1

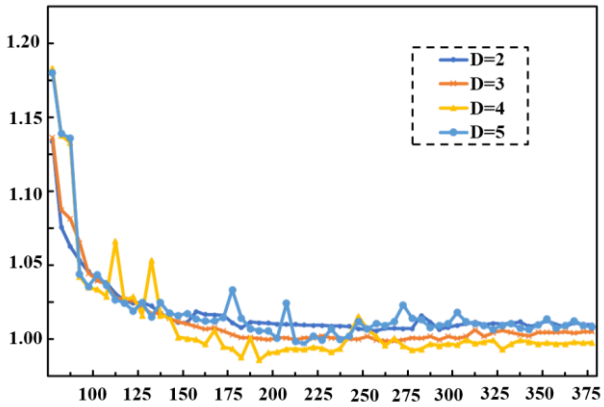

Figure 10: Estimation performance comparison of XGBoost with different max_depth and n_estimator parameters

Figure 11 demonstrates the extent to which the estimation performance of XGBoost on the test samples is affected by changes in the n_estimator and max_depth parameters. It can be seen that the average absolute errors of the XGBoost models with different max_depth settings are relatively large when the n_estimator is small, and after 200 iterations, the curves all start to

Gradually converge, in addition, it can be seen that at n estima1or equal to 200, the model estimation performance is not significantly improved with the increase of the number of layers, therefore, to limit the complexity of the model and prevent overfitting, the optimal values of n_estimator and max_depth are set to 200 and 3 layers, respectively.

4.3 Analysis of estimated results

Compared to traditional methods, the XGBoost-based INL estimation model is more accurate, but less interpretable and almost a black-box model. Shapley Additive explanations (SHAP), based on game theory and able to quantify the marginal contribution of each feature to the model output value, is a widely applicable framework for model interpretation [29]. Therefore, this work employs SHAP to quantify the influences on INL in the model and enhance the interpretability of the model. The use of PCA and statistical descriptors as input features is consistent with recent unsupervised learning and feature reduction methodologies in embedded signal analysis [30].

According to the feature importance ranking given by the SHAP model interpreter, the features with the lowest importance (including variables such as INL-kurt, DNL-std, DNL-mean, etc.) were eliminated one by one to reduce the complexity of the model. In addition, this work discusses the principal component vectors included in the model, as shown in Figure 11. When the model incorporates 48 principal component features, the model has the lowest absolute error and the best estimation performance on the test set.

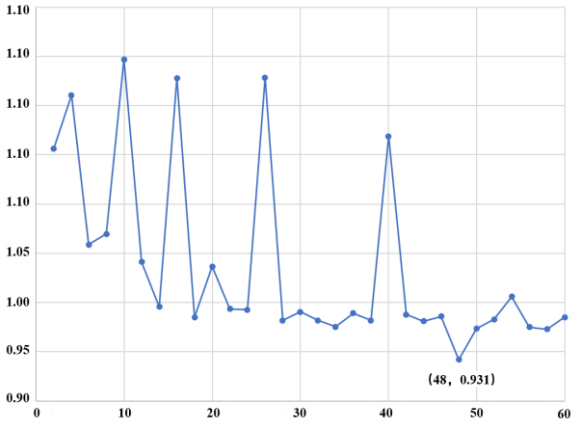

Figure: 11 Comparison of estimation performance of XGBoost model when taking the first n principal components

Figure 12 shows the estimated and measured values of XGBoost in the test set (100 samples are randomly selected here to demonstrate the effect), where the dashed line indicates the model estimated values, the solid line indicates the measured values and the horizontal axis is the sample number. It can be seen that the trend of the measured values and the model-estimated values are generally consistent. Tabel 3 demonstrates the quantitative analysis of XGBoost's estimation results for all test samples (512 sets), and it can be seen that there are only 31 sets of samples with estimation errors greater than 3 Db, accounting for 7% of the test set weight, i.e., 92% of the data have errors within the range of 3 Db.

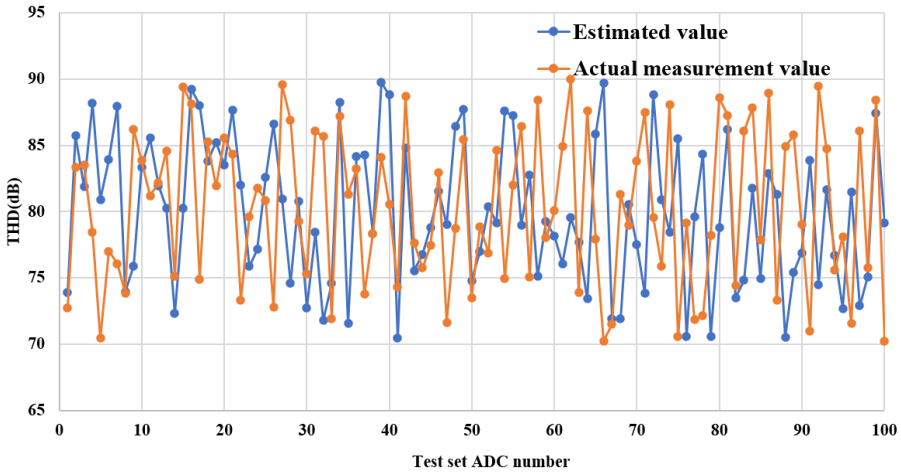

Figure 12: THD estimate vs. reference value

Table 3: Analysis of XGBoost estimation error in the test set

Error (Db)	Points	Proportion in the test set
±2	436	85%
±3	477	92%
±4	502	97%

Figure 13 shows the top 10 features with the highest contribution (SHAP value) to the estimation results, with the features ranked from top to bottom according to their contribution. It can be seen that the gain error, with a SHAP value equal to about 0.008, has the highest contribution to the total harmonic misalignment parameter, significantly higher than the second-ranked INL-RMS (with a SHAP value equal to about 0.004). From the second NL-RMS to PCA-12 (SHAP value | approximately equal to 0.003), the contributions of several characteristic variables show a steady decreasing trend. In addition, it is easy to find that nine of the top ten feature variables with the highest SHAP values originate from the integral nonlinear curve, which implies that the INL curve is an important feature for estimating the THD parameter, a conclusion that is consistent with the findings of J.B. Duan et al. in the literature the results of the study are consistent.

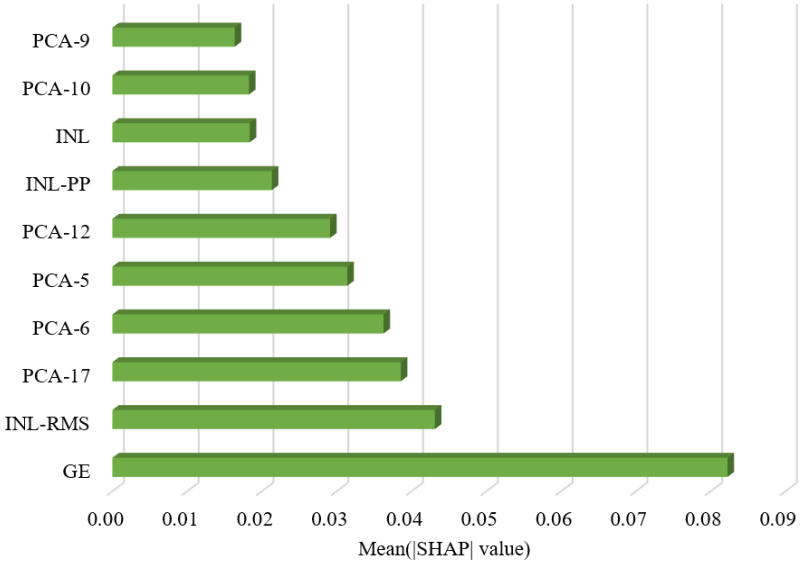

Figure 13: Mean (|SHAP values|) for the 16 features that have the greatest impact on the THD estimates.

5 System software design

5.1 FFT algorithm principle

N*logN times operation, significantly improving the arithmetic process reduces the amount of arithmetic[32]. Fast Fourier transform according to the discrete Fourier transform of the parity of the real and other characteristics, the use of symmetry, constantly divided into two methods, close to the limit, that is, divided into two and two groups of DFT operation unit, the algorithm complexity is optimized for the O (N * logN) level, as a way to greatly reduce the computer's running time.

The bisection algorithm is as follows:

$$X_k = \sum_{n=0}^{N-1} x_n e^{\frac{-i2\pi kn}{N}} = \sum_{m=0}^{N-1} x_{2m} e^{\frac{-i2\pi k(2m)}{N}} + \sum_{m=0}^{N-1} x_{2m+1} e^{\frac{-i2\pi k(2m+1)}{N}} = \sum_{m=0}^{N-1} x_{2m} e^{\frac{-i2\pi k(2m)}{N/2}} + \sum_{m=0}^{N-1} x_{2m+1} e^{\frac{-i2\pi km}{N/2}}$$

5.2 FFT program implementation

As the FFT microprocessor uses machine language, machine language through the complementary code to complete the operation [31]-[32], the output data for the complementary code, and the need for the original code through the complementary code of the relationship between the program to get the desired results. When the output is positive, the complementary code and the original code are equal, the output is negative, the highest bit of the complementary code is unchanged, and the rest of the inverse of each of the original code, through the highest bit of data to determine the number of positive and negative, the highest bit of 1 that is, for the negative, for the 0 that is, for the positive number. In the finalized platform, the FFT algorithm is executed on the host PC using optimized scientific computing libraries such as NumPy, based on raw data collected by the FPGA. Earlier prototypes implemented FFT logic at the microcontroller level for validation purposes, but these were superseded by software-based methods offering higher resolution and performance. Through the above operations can be obtained after the true value of the data. The program block diagram is shown in Figure 14.

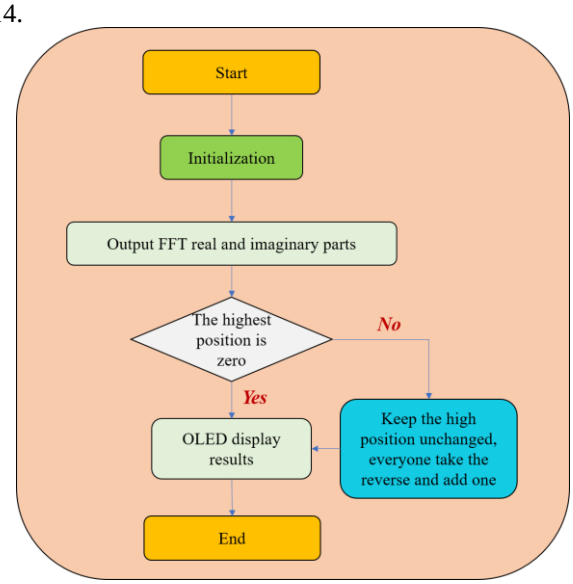

Figure 14: Program block diagram

Before building the system, first debug individual modules to work properly, after all the modules can meet the requirements, start building the system, the power amplifier circuit, non-contact current sensor, and microcontroller detection circuit are fixed in the PCB board, and will be connected to fix the wires, connected to the switching power supply and the signal generator, the system indicators are tested in turn.

The following table shows the test data when the input signal is sinusoidal, and the data are the average value obtained from five measurements.

Table 4: Sine wave test data sheet

Input of signal A		Output of signal B		Amplitude error	Frequency error
A/V	A/Hz	Output peak to peak value /V	Output frequency /Hz		
1.50	50	1.44	50.51	4.75%	0.020%
2.50	100	2.42	101.02	4.04%	0.020%
5.00	200	4.87	202.01	3.64%	0.005%
6.50	500	6.41	505.04	2.32%	0.008%
8.00	700	7.99	707.08	1.31%	0.014%
9.00	900	9.16	908.99	0.79%	0.001%

The results presented in Table 4, which detail the amplitude and frequency errors observed during sinusoidal signal testing, offer an indirect yet important reflection of the system's overall ADC testing precision. The amplitude error affects the linearity of the ADC's transfer function, which directly correlates with the effective number of bits (ENOB) and total harmonic distortion (THD). For example, under the input signal of 5.00 V and 200 Hz, the amplitude error was maintained within 3.64%, while the frequency error remained as low as 0.005%. Such low deviations in both amplitude and frequency ensure that the excitation signal maintains spectral purity, which is crucial for accurate dynamic performance estimation.

These stable signal conditions form a reliable basis for FFT analysis and the XGBoost regression model, enabling precise estimation of THD and signal-to-noise ratio (SNR). The observed consistency between the hardware-generated signal and the measured output confirms the system's capability to preserve signal integrity. This, in turn, validates the reliability of subsequent dynamic performance metrics, as reflected in the experimental results where over 85% of test samples achieved THD estimation errors within ±2 dB and ENOB deviation within ±0.5 bits. Therefore, the low signal distortion reported in Table 4 is not only a reflection of hardware precision but also a prerequisite condition that contributes to the high accuracy of the overall ADC evaluation process.

6 Discussion

The proposed ADC test platform demonstrates considerable advantages over traditional evaluation methods in terms of performance, flexibility, and implementation cost. As summarized in Table 1, conventional approaches for ADC testing—such as histogram-based static tests and FFT-based dynamic analyses—often require specialized hardware configurations and are limited in their ability to adapt to varying signal conditions. In contrast, our platform integrates low-cost hardware components with a machine learning-based dynamic parameter estimation algorithm, achieving accurate and consistent results across a range of test scenarios. The experimental results indicate that the proposed system can estimate total harmonic distortion (THD) with errors within ±2 dB for 85% of the test samples and within ±3 dB for 92%, while maintaining the effective number of bits (ENOB) deviation within ±0.5 bits. These results highlight the system's capability to perform both static and dynamic testing with high precision.

A key contribution of this work is the integration of the XGBoost regression model for dynamic parameter estimation. Compared to traditional analytical or FFT-only methods, XGBoost exhibits enhanced robustness and adaptability when mapping complex nonlinear relationships between static ADC characteristics (such as INL and DNL) and dynamic performance metrics. The use of SHAP (SHapley Additive exPlanations) further improves model transparency by quantifying the contribution of each feature to the final output, which supports the interpretability of the prediction process. Notably, principal components derived from INL curves emerged as the most influential features, confirming the theoretical link between static nonlinearity and dynamic spectral performance.

While the system achieves promising results, certain trade-offs must be acknowledged. The inclusion of amplification and filtering circuits adds some complexity to the hardware design, and although the overall latency introduced by the FFT and XGBoost pipeline is relatively small, it may still be a consideration in time-critical applications. Furthermore, despite the improvements in model interpretability via SHAP, machine learning models inherently involve a level of abstraction that can complicate result verification compared to fully analytical methods.

Nonetheless, the developed platform provides a compelling solution for high-precision ADC testing in both academic and industrial contexts. It offers a balance between cost, accuracy, and extensibility, and can be adapted to a range of testing requirements. Future work will focus on extending the platform to support higher-resolution ADCs, multi-channel acquisition, and real-time model acceleration through FPGA-based

deployment, thereby further enhancing its applicability in advanced signal processing environments.

7 Conclusion

This paper presents the design and implementation of a high-precision ADC (analog-to-digital converter) test platform that integrates hardware and software to comprehensively evaluate the static and dynamic performance of ADCs. The main contributions of this work are summarized as follows:

Hardware Design: The hardware platform is built using the STC12C5A60S2 microcontroller and the AD9833 chip, combined with the design of amplification and filtering circuits, to construct a high-precision data acquisition and processing system. Experimental results demonstrate that the platform accurately extracts key ADC performance metrics, validating the effectiveness and reliability of the system design. In the future, the platform can be further optimized to support higher precision testing requirements and expanded application scenarios, providing technical support for ADC development and quality control.

Experimental validation confirms that the signal generator module produces stable excitation signals, while the XGBoost-based dynamic parameter estimation model achieves high accuracy in predicting key ADC performance metrics such as THD and ENOB. This demonstrates the platform's capability for accurate ADC evaluation in both static and dynamic contexts.

Static and Dynamic Parameter Extraction: A manual static performance parameter extraction method is proposed by integrating time series analysis and principal component analysis. Experimental results indicate that the model estimation based on this method significantly outperforms models using traditional static parameters as input features. Furthermore, all feature variables used in the model can be obtained during static parameter testing, ensuring the model's applicability in production testing. Additionally, the XGBoost model is selected for ADC dynamic parameter estimation. The comparative analysis of estimation performance among different models reveals that the XGBoost model achieves superior estimation accuracy. These results demonstrate the potential of the proposed platform and methods to enhance ADC performance evaluation and contribute to the advancement of ADC technology.

References

[1] Massaro, A. (2023). Advanced electronic and optoelectronic sensors, applications, modelling and industry 5.0 perspectives. Applied Sciences, 13(7), 4582. https://doi.org/10.3390/app13074582

[2] Huang, R., Yan, P., & Yang, X. (2021). Knowledge map visualization of technology hotspots and development trends in China's textile manufacturing industry. IET Collaborative Intelligent Manufacturing, 3(3), 243-251. https://doi.org/10.1049/cim2.12024

[3] Li, Q., Yang, Y., & Jiang, P. (2022). Remote monitoring and maintenance for equipment and production lines on industrial internet: A literature review. Machines, 11(1), 12. https://doi.org/10.3390/machines11010012

[4] Wu, G., Chen, Z., & Dang, J. (2024). IoT Sensing Technology. In Intelligent Bridge Maintenance and Management: Emerging Digital Technologies (pp. 67-105). Singapore: Springer Nature Singapore. https://doi.org/10.1007/978-981-97-3827-4_3

[5] Fu, B., Liu, Y., Li, Y., Wang, C., Li, C., Jiang, W., ... & Zhao, W. (2021). The research priorities of resources and environmental sciences. Geography and Sustainability, 2(2), 87-94. https://doi.org/10.1016/j.geosus.2021.04.001

[6] McNutt, M. K. (2022). Civilization-saving science for the twenty-first century. Annual Review of Earth and Planetary Sciences, 50(1), 1-12. https://doi.org/10.1146/annurev-earth-033021-081125

[7] Waho, T. (2022). Introduction to Analog-to-Digital Converters. River Publishers. https://doi.org/10.1201/9781003338680

[8] Wang, J., Ilyas, N., Ren, Y., Ji, Y., Li, S., Li, C., ... & Ang, K. W. (2024). Technology and integration roadmap for optoelectronic memristor. Advanced Materials, 36(9), 2307393. https://doi.org/10.1002/adma.202307393

[9] Licastro, D. (2022). Development and evaluation of Synthesis and Optimization strategies for digital integrated circuits (Doctoral dissertation, Politecnico di Torino). http://webthesis.biblio.polito.it/id/eprint/24515

[10] Vaikkola, V. P. (2024). Integrated Circuit Testing Using Automatic Test Equipment.

[11] Wei, L., Junfeng, C., & Shiguang, S. (2023, October). ADC Static Test System Based on LabVIEW Platform. In 2023 8th International Conference on Integrated Circuits and Microsystems (ICICM) (pp. 387-391). IEEE. https://doi.org/10.1109/ICICM59499.2023.10365768

[12] Sparta, R. (2024). Implementation and testing of modular ADCS software using modular avionics test bench for cubesats (Doctoral dissertation, Politecnico di Torino). http://webthesis.biblio.polito.it/id/eprint/31327

[13] Duan, J., & Chen, D. (2011, May). SNR measurement based on linearity test for ADC BIST. In 2011 IEEE International Symposium of Circuits and Systems (ISCAS) (pp. 269-272). IEEE. https://doi.org/10.1109/ISCAS.2011.5937553

[14] Janik, J. M., & Fresnaud, V. (2007). A spectral approach to estimate the INL of A/D converter. Computer Standards & Interfaces, 29(1), 31-37. https://doi.org/10.1016/j.csi.2005.12.004

[15] Duan, J., Jin, L., & Chen, D. (2012). Testing ADC spectral performance without dedicated data acquisition. IEEE Transactions on Instrumentation and Measurement, 61(11), 2941-2952. https://doi.org/10.1109/TIM.2012.2202949

[16] Ciofi, C., & Neri, B. (2003, May). Low-frequency noise measurements: applications, methodologies and instrumentation. In Noise in Devices and Circuits (Vol. 5113, pp. 350-367). SPIE. https://doi.org/10.1117/12.489652

[17] Van de Plassche, R. J. (2012). Integrated analog-to-digital and digital-to-analog converters (Vol. 264). Springer Science & Business Media. https://doi.org/10.1007/978-1-4615-2748-0

[18] Hou, N., Song, W., Zhu, Y., Sun, X., & Li, W. (2018). Dynamic and static performance optimization of dual active bridge DC-DC converters. Journal of Modern Power Systems and Clean Energy, 6(3), 607-618. https://doi.org/10.1007/s40565-017-0343-7

[19] Ambardar, A. (1995). Analog and digital signal processing (p. 700). Boston, MA, USA: PWS.

[20] Chen, D., Cui, X., Zhang, Q., Li, D., Cheng, W., Fei, C., & Yang, Y. (2022). A survey on analog-to-digital converter integrated circuits for miniaturized high resolution ultrasonic imaging system. Micromachines, 13(1), 114. https://doi.org/10.3390/mi13010114

[21] Verma, A., & Saini, B. S. (2024, February). Comparative Analysis and Review of ADCs and Comparators for Use in Biomedical Applications. In 2024 2nd International Conference on Computer, Communication and Control (IC4) (pp. 1-6). IEEE. https://doi.org/10.1109/|C457434.2024.10486271

[22] Georgoulopoulos, N., Mamali, T., & Hatzopoulos, A. (2024). Design and Verification of a SAR ADC SystemVerilog Real Number Model. Journal of Electronic Testing, 40(3), 315-328. https://doi.org/10.1007/s10836-024-06124-8

[23] Feng, B., Mera, A., & Lu, L. (2020). {P2IM}: Scalable and hardware-independent firmware testing via automatic peripheral interface modeling. In 29th USENIX Security Symposium (USENIX Security 20) (pp. 1237-1254). https://doi.org/10.5555/3489212.3489282

[24] Navabi, Z. (2011). Digital system test and testable design. Springer. https://doi. org/10.1007/978-1-4419-7548-5.

[25] Egea, X., Sanchis, E., González, V., Gadea, A., Blasco, J. M., Barrientos, D., ... & Wadsworth, R. (2012, June). Design and test of a high-speed flash ADC mezzanine card for high-resolution and timing performance in nuclear structure experiments. In 2012 18th IEEE-NPSS Real Time Conference (pp. 1-8). IEEE. https://doi. org/10.1109/RTC.2012.6418150

[26] van den Hoven, R. A. T. (2006). A pre-correction method for improved static linearity using parallel DACs.

[27] Chen, T., & Guestrin, C. (2016, August). Xgboost: A scalable tree boosting system. In Proceedings of the 22nd acm sigkdd international conference on knowledge discovery and data mining (pp. 785-794). https://doi.org/10.1145/2939672.2939785

[28] Sun, X., Lin, Y., & Yin, Q. (2025). Digital control circuit of accelerometer in gravity measurement with PSO optimized ADC-DSP integration. Informatica, 49(1), 109–116. https://doi.org/10.31449/inf.v49i23.8444

[29] Š trumbelj, E., & Kononenko, I. (2014). Explaining prediction models and individual predictions with feature contributions. knowledge and information systems, 41, 647-665. https://doi.org/10.1007/s10115-013-0679-x

[30] Chefrour, H. (2021). Unsupervised deep learning: Taxonomy and algorithms. Informatica, 45(1), 21–32. https://doi.org/10.31449/inf.v46i2.3820

[31] Swartzlander, E. E., & Goto, G. (2017). Computer arithmetic. In Digital Design and Fabrication (pp. 11-1). CRC Press. https://doi.org/10.1201/9780849386046-11

[32] Lee, Y. C., Chan, Y. K., & Koo, V. C. (2021). Design and Implementation of Field-Programmable Gate Array Based Fast Fourier Transform Co-Processor Using Verilog Hardware Description Language. Progress In Electromagnetics Research B, 92. https://doi.org/10.2528/PIERB20122806